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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/605,312	06/28/2000	Andrew J. Wright	0325.00353	6231

21363 7590 03/11/2004

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EXAMINER	
CHO, JAMES HYONCHOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/605,312	WRIGHT, ANDREW J.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5 and 18-20* is/are allowed.

6)☒ Claim(s) *6 and 13-15* is/are rejected.

7)☒ Claim(s) *7-12,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6-8-2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 2, 2004 has been entered.

Drawings

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on February 2, 2004 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the AND plane configured to generate a product term in response to a plurality of product term inputs recited in claims must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 6 and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Turner et al. (US PAT No. 4,879,688).

Regarding claim 6, Fig. 21 of Turner et al. teaches an apparatus or a method for providing a product term input of a programmable logic device comprising an AND plane (455) configured to generate a product term (output coupled to 510a-517a) in response to a plurality of product term inputs (signals coupled to 455 via drivers coupled to /Q of 510a), a first circuit (driver) configured to present a first value stored in a first memory cell (data stored in 510a) as one of the plurality of product term inputs in response to a first state of an input signal (Clock input to 510a); and a second circuit (driver coupled to 511a) configured to present a second value stored in a second memory cell (data stored in 511a) as one of the plurality of product term inputs in response to a second state of an input signal (Clock input to 511a where clock input to 510a and 511a are the same), where the first and second stored values are programmable during configuration of the apparatus (col. 22, lines 36-64).

Regarding claim 13, Fig. 21 of Turner et al. teaches the apparatus according to claim 6 where the apparatus comprises a programmable logic device (ABSTRACT).

Regarding claim 14, Figs. 7 and 21 of Turner et al. teaches the apparatus according to claim 6, further comprising a group of gates (Fig. 7; col. 7, lines 44-55) configured to generate a sum-of-products terms in response to a plurality of product terms, where the AND plane is further configured to generate the plurality of product terms.

Regarding claim 15, Fig. 21 of Turner et al. teaches the apparatus according to claim 6, where the input signal comprises an input term (Clock signal is an input term for 510a and 511a).

Allowable Subject Matter

5. Claims 1-5 and 18-20 are allowable over the prior art of record.

6. Claims 7-12 and 16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims as well as including all corrections of claim objection stated above.

The following is a statement of reasons for the indication of allowable subject matter: Although, TURNER ET AL. discloses an in-system programmable logic device, TURNER ET AL. differs from the present claimed invention because, among other things, TURNER ET AL. pertains to configuring and reconfiguring while installed in a user's system, whereas the present claimed invention pertains to a programmable logic device having a first and second memory cell directly coupled to an input terminal of a

first transmission gate and an input terminal of a second transmission gate respectively. In the present claimed invention, the first and second transmission gates are configured to couple the first and second memory cell to an input terminal of the AND plane and the input signal is coupled to a control terminal of the first and second transmission gates. Accordingly, one of ordinary skill in the art would not have been motivated to modify the teachings of TURNER ET AL. to meet the claimed limitation as set forth in the present claimed invention.

Response to Arguments

7. Applicant's arguments with respect to claims 6 and 13-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takata et al. (US PAT No. 4,992,679) discloses a programmable logic device with multiple independent feedbacks per input/output terminal.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

February 24, 2004